CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. An integrated circuit including
a patterned copper layer,
a patterned aluminum layer,
a stud connection in an opening between a location on said patterned copper layer and a location on said patterned aluminum layer, and
a liner in said opening and extending between said stud connection and said location on said patterned copper layer.

2. An integrated circuit as recited in claim 1 wherein said liner comprises
a layer of tantalum nitride, and
a layer of PVD tungsten.

3. An integrated circuit as recited in claim 1 wherein said liner comprises
a layer of titanium, and
a layer of titanium nitride or PVD tungsten.

4. An integrated circuit as recited in claim 1 wherein said stud connection is formed of tungsten.

5. An integrated circuit as recited in claim 1 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

6. An integrated circuit as recited in claim 2 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

7. An integrated circuit as recited in claim 3 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

8. An integrated circuit as recited in claim 4 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

9. An integrated circuit as recited in claim 1, further including a covering layer.

10. An integrated circuit as recited in claim 9 wherein said covering layer includes a layer of silane-based high density plasma oxide.

11. A method of forming an interface structure between copper and aluminum metallurgy layers in an integrated circuit, said method comprising steps of

covering a copper metallurgy layer with an insulator,

forming an opening through said insulator to said copper metallurgy layer,

forming a liner of a conductive barrier material in said opening, and

filling a remainder of said opening with a conductive material to form a stud, and

forming a patterned aluminum metallurgy layer over said stud.

12. A method as recited in claim 11, wherein said step of forming a liner includes the further steps of chemical vapor deposition of tantalum nitride and tungsten, respectively.

13. A method as recited in claim 11, including the further step of

forming a covering layer over said patterned aluminum layer.

14. A method as recited in claim 14, wherein said covering layer includes a layer of silane-based high density plasma oxide.

15. A method as recited in claim 11, wherein said patterned aluminum layer includes interconnects and solder or wire bond connection pads, said method including the further step of

opening said covering layer at a said solder or wire bond connection pad.

16. A method as recited in claim 11, including the further step of forming a barrier layer over said copper metallurgy layer.